DESIGN AND ANALYSIS OF LOW POWER VLSI BASED SRAM CELL USING CMOS, FINFET AND GNRFET TECHNOLOGIES

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Abstract - Graphene nanoribbon field-effect transistors (GNRFETs) has the ability to be processed and fabricated on a massive scale, making them a viable device for beyond-CMOS nanoelectronics. The primary focus of this study is the design of an SRAM cell using 10 transistors and taking into account two different threshold values. Research efforts centered on FinFET and GNRFET during circuit design. Despite claims of higher performance, lower power consumption, and identical reliability at comparable operating points to scaled CMOS circuits, simulation studies demonstrate that GNRFET circuits are more susceptible to variations and errors. The device and CAD groups working with graphene have some difficult engineering, modeling, and simulation problems to solve as a consequence of these results.
Keywords: CMOS, GNRFET, VLSI, SRAM, HSpice.

1 INTRODUCTION

Increasing transistor functionality, decreasing power dissipation, and decreasing costs have all been possible thanks to downsizing of semiconductor devices, which has become a driving force in the growth of electronics. In 1965, Intel co-founder Gordon Moore proposed Moore's Law, which states that the number of transistors on a chip will nearly double every two years. With the advent of smaller feature sizes, the semiconductor industry has made enormous gains in recent decades, leading to an increase in the number of transistors per chip. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have become crucial to the modern Very Large Scale Industry due to the Moore's Law-driven miniaturization of transistors (VLSI). The size of the MOSFET has decreased from multiple microns to 32 nm or smaller in the last two decades. Short channel effects, drain induced barrier lowering, threshold voltage drop, etc., have begun to affect performance as MOSFET feature sizes continue to shrink. Reduced gate oxide thickness increases leakage current, which slows down the device and increases power consumption. MOSFETs act erratically down in the nanometer region. In recent years, researchers have looked into a wide variety of novel nanotechnology devices, including the field-effect transistor (FinFET), metal-oxide-semiconductor field-effect transistor (MOSFET), carbon nanotube field-effect transistor (CNTFET), graphene nanoribbon field-effect transistor (GNRFET), etc., to address these issues.

Microelectronic memory made of semiconductors are among the most crucial parts of any digital logic system design, including computer-based applications. Large amounts of digital information, necessary for all digital systems, can be stored in semiconductor memory arrays. Storage functions require a larger number of transistors than logic operations or other uses, although the amount of memory needed in a given system is application-specific. Memory and fabrication technologies have advanced in the direction of greater data storage densities to keep up with the ever-increasing need for vast amounts of storage space. The capacity of commercially accessible single-chip read/write memories has reached 1 GB, and on-chip memory arrays are now frequently employed as subsystems in VLSI circuits. Data storage and retrieval methods are the two main categories under which semiconductor memory falls. The bits of information stored in a computer's RAM must be able to be read, written, and accessed whenever necessary (RAM). This data is just for a limited time. SRAM is a great choice for cache memory in microprocessors, mainframes,

engineering workstations, and portable devices because of its high speed and low power consumption. Memory cells are often constructed using transistors. Moore's law states, basically, that the total number of transistors employed on a single device will grow at an exponential rate. Despite having rapid operating speeds, smaller leakage, and fewer transistors, their efficiency starts to drop below 32nm. The International Technological Roadmap for Semiconductors provides a comprehensive overview of the semiconductor industry's most recent breakthroughs and market trends (ITRS).

New generations of high-performance VLSI devices need for innovative approaches to storing digital information directly on the silicon. The best of these solutions are SRAMs. Many different kinds of microelectronic devices would not function without SRAMS. The increasing pressure from consumers to shrink their electronics has led to this trend. The usage of sub 10nm MOSFETs in very large-scale integrated (VLSI) circuit design is increasingly constrained as a result of issues including susceptibility to process changes and an increase in transistor leakage brought about by scaling. The leakage currents have become a significant obstacle now that scaling has reached a critical apex. These findings call for the development of an entirely new FET system. Graphene's introduction has provided a friendly response to such needs.

Graphene nanoribbon field-effect transistors (GNRFETs) have the ability to be processed and fabricated on a massive scale, making them a viable device for beyond-CMOS nano electronics. Based on atomistic quantum-transport modeling and circuit simulation, experts in the field of GNRFETs have shown that, at equivalent operating conditions, GNRFETs beat scaled CMOS by a factor of over 26-144 in terms of the energy delay product. In addition, the functionality and dependability of GNRFET circuits are analyzed quantitatively in [1], which details the effects of variations and faults. Despite its promise of improved performance, reduced energy consumption, and identical reliability at similar operating points, the simulation results of [1] reveal that GNRFET circuits are more prone to variations and defects than scaled CMOS circuits.

2 PROPOSED SYSTEM

Methodology

FinFET

One sort of nanoscale technology that can replace conventional complementary metal-oxide-semiconductor (CMOS) technology is the fin-type field-effect transistor (FinFETs). Devices with FinFETs have two gates. A FinFET's performance can be improved by shorting its two gates, while leakage and the number of transistors required can be minimized by controlling the gates separately [28, 29].

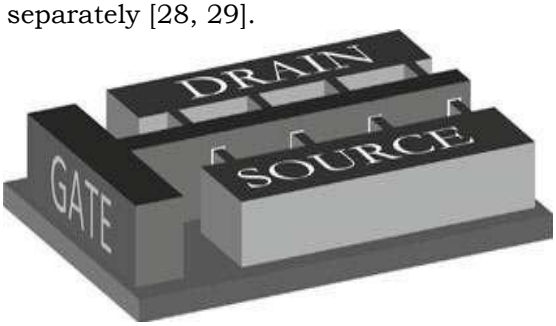

Fig 1: Multi-fin FinFET

The FinFET chip's gate electrodes surround a wafer-thin silicon core. By relocating the gate electrode to the bottom of the channel, the FinFET enables front and rear gates to be separately controlled. When n is the total number of fins and h is the total height of the fins, the effective gate width of a FinFET is 2nh. Hence, more fins enable wider transistors that can sustain higher on-currents.

Carbon Nanotubes

Nanotubes made of carbon atoms are cylindrical in shape and exhibit unusually high levels of mechanical, electrical, thermal, optical, and chemical capabilities. Carbon nanotubes come in two different types: Each with one or more walls. Carbon nanotubes (or arrays of them) serve as the channel material in a CNTFET (Carbon Nanotube Field Effect Transistor), rather than the bulk silicon used in a MOSFET. [30-32]

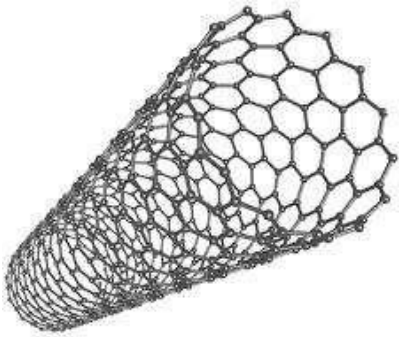

Fig 2: Carbon Nanotube Structure

The nanotubes' folding angle and diameter determine whether they are metallic or semiconductive. Semiconducting nanotubes have a decreasing band gap as their diameter increases. Carbon nanotubes, due to their unique electronic structure, are promising candidates for innovative molecular devices. To get beyond the limitations of CMOS technology, this can be employed even after the 32nm node is reached.

Graphene Nanoribbon

Graphene nanoribbons, also called nano-graphite ribbons, are very long, very thin sheets of graphene (often thinner than 50 nm). To study the impact of graphene's edges and nanoscale size, Mitsutaka Fujita and co-authors developed the concept of graphene ribbons as a theoretical model. Graphene nanoribbons (GNRs) are the result of a careful patterning process in which graphene is laterally restricted in a ribbon-like form [33–35].

They come in two distinct styles, armchair and zigzag. Each zigzag section has a different angle than the one before it. Each set of two armchair segments is a 120-degree rotation from the set before it. Non-bonding molecular orbitals close to the Fermi energy are transferred from the zigzag edges to the edge localized state. Large shifts in their optical and electrical properties are predicted as a result of their quantization.

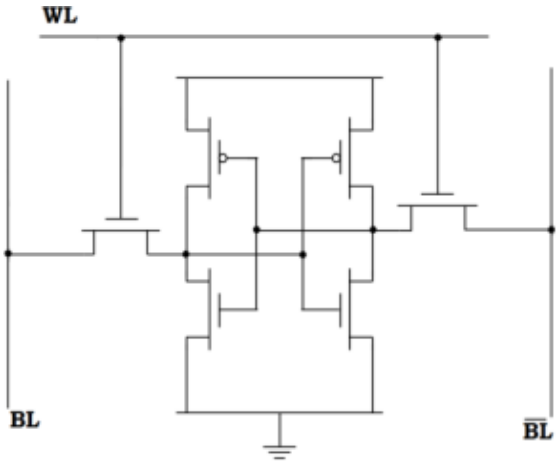

Fig.3 Graphene Nanoribbon

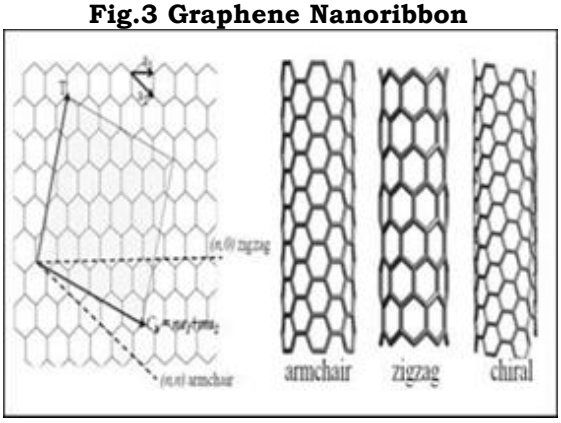

Fig 4: 6T SRAM Cell

10T SRAM Cell With Dual Threshold

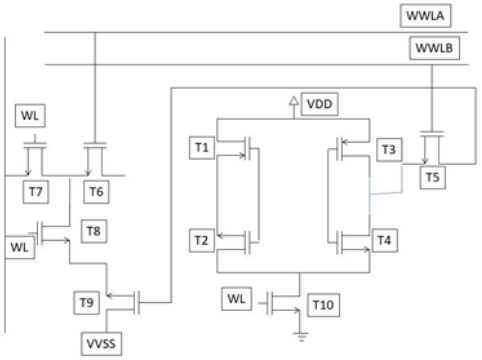

Fig 5: Proposed GNRFET 10T SRAM cell with dual Threshold

Read/write conflicts reduce the performance and reliability of regular 6T SRAM. A dedicated read wordline (RWL) is needed to minimize read interruption in 8T SRAM cells since the write bitline and the read bitline are physically separated. By forcing charges from the bitline into the internal node of the 8T SRAM cell, the write wordline (WWL) causes a half-select problem during interleaving column sharing. As more memory cells were added to the bitline, the half-select issue

became more severe. SRAM memory cells that employ a single-ended approach considerably reduce power consumption. It helps minimize the amount of leakage current and the overall size of the chip. Using this single-ended method, the dynamic active can be cut in half. Yet the read/write delays in SRAM cells are more noticeable when the supply voltage is low. Many solutions have been proposed to deal with these issues, including feedback read/write assist, asymmetrical read/write -assist, dual-threshold voltage, cross-point data awareness, and power boost. In this study, we present a novel single-ended GNRFET-based 10T SRAM cell. A sample circuit diagram for a 9T SRAM cell using GNRFETs is shown in Fig. 6. In the suggested cell, data is stored at node Q by means of two cross-coupled inverters, inv1 (T1 and T2), and at node Qn by means of two inverters, inv2 (T3 and T4). The intended 9T SRAM cell can be made more efficient by the addition of a dedicated read/write interface (T5-T9). The new 10T SRAM cell outperforms the 8T SRAM cell by a factor of 2.8 in read disturb immunity with just a 1.2 increase in area need thanks to its dedicated read port (T7, T8 and T9). SRAM chips' write capacity and cell stability have been enhanced by optimizing the ratio of transistor sizes (T5/T9) in the write port to 1.8. Bit-interleaving is a technique used to improve soft-error rates and reduce coupling-noise levels. Using a high cell count on a single bit line, the row-column select line increases array throughput while decreasing area overhead.

3 PROPOSED 14T SRAM CELL

Finally, in CMOS development, the standard 6T and 10T SRAM cells are used as the primary storing component and an essential part of PC layouts and architecture. Read/make conflict, the half-select unsettling impact, and read upset are all present in the immediately arranged 6T SRAM with a massive breaking point limit [27]. The standard Si-CMOS SRAM cell's reliability drops precipitously at low stock voltage due to VMIN requirements, which fully corrupts with supply voltage scaling and its display effect [27].

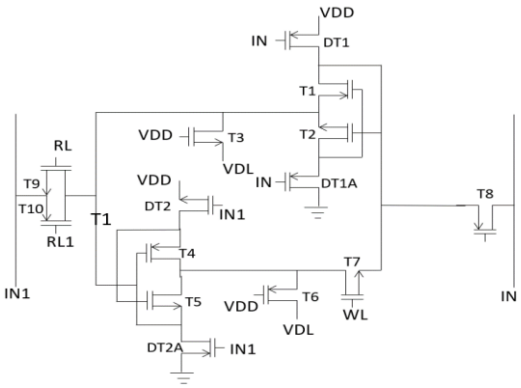

Fig 6: 14T SRAM cell with dual Threshold and modified Lector Approach

Typical 6T SRAM cells are used as the primary memory component in the development of CMOS computers. Read/make conflict, the half-select unsettling impact, and read upset are all present in the immediately arranged 6T SRAM with a massive breaking point limit [27]. When the supply voltage is lowered, the reliability of a standard Si-CMOS SRAM cell deteriorates, which in turn affects the exhibit in a negative way because of the VMIN requirements [28]. Some researchers [28-30] have suggested honing one's courage and carrying out a low-force SRAM plan at a low store voltage. Read maintains can be used to strengthen the read security of many SRAM cells, as they effectively update the read steamed to make read SNM indistinguishable from hold SNM [29-31]. Strength of pull down to pass entrance and surrender entrance to pull, freely, are refreshed; covered digit line, negative-VSS, and word-line-under-drive are utilized to enhance read tasks; negative-cycle line, word-line-over-drive, and transient-voltage-breakdown are utilized to enhance make tasks; and isolating is utilized to enhance make tasks. When it comes to read security, a disproportionate SRAM cell's single read port and increasing pull-down strength are key factors in reducing read upset [35]. Read upset persists despite efforts to mitigate it via the information system, which have yielded a fundamental improvement in consistency via the limitation of telephone collection efforts with respect to read bitline. Gliding focal point storage is activated by the NMOS semiconductors used in the study, which influences

spilling current in the subthreshold region and may, in turn, initiate delicate mess up and varied cell upset [36]. Using the piece interleaving strategy with fumble check and adjustment [37], you may limit the disruption to the various cells. Picked wordline (WL) conduct pseudo read development drains power, making the typical 6T SRAM cell inappropriate for digit interleaving architecture [38, 39]. When applied to both line and segment based structures, wordline (WL) planning eliminates the make half-select uncomfortable affect that reduces write ability.

4 RESULTS

Graphene nanoribbon field effect transistors (GNRFETs) are an exciting development in the realm of nanoelectronics. Since GNRFETs are scalable and free of the chirality issues that plague CNTFETs, they are the superior technology. Non-alignment and similar issues with CNTFETs, which have a cylinder form, are eliminated through the use of transfer-free, in situ GNRFET development that is compatible with silicon. Monolayer graphene sheets with a narrow bandgap can be arranged in a specific transport channel orientation to create graphene nanoribbons (GNR). The unique electrical properties and high mobility of GNRFETs are the result of the material adopting the properties of both graphene and CNTs. It can carry a lot of current while being relatively cool and producing little heat. Graphene has excellent switching properties and is a good heat conductor. The bandgap of GNRFETs can be adjusted, allowing them to take on either a metallic or semiconducting state. Based on its increased mobility and current carrying capability, a GNRFET dissipates less power than FinFET and CNTFET based designs, according to a performance evaluation research published in [1].

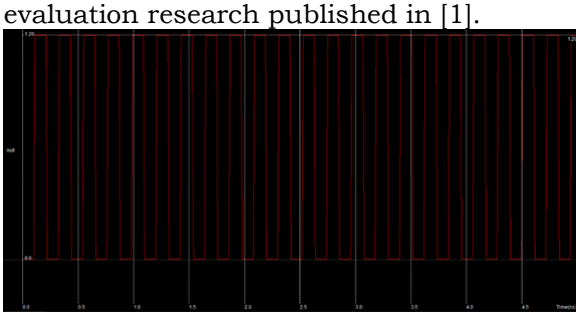

Fig 7 (a)Timing Diagram

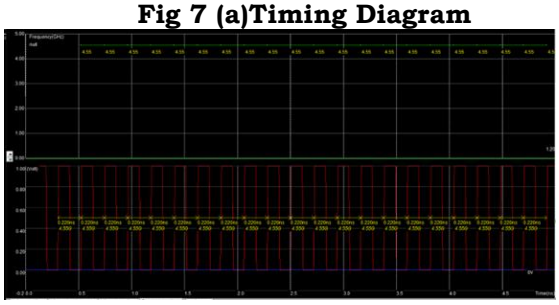

Fig 7 (b) Timing Diagram

Table 1 Comparison with FinFET and CMOS of 14T SRAM Cell 1 bit

S.NO.	NM	Power in mW for CMOS	Power in mW for FinFET	Power in nW for GNRFET
1	22	6.08	3.57	2.49
2	14	5.32	3.28	-
3	10	5.76	2.67	-
4	7	5.68	2.53	-

Table 2: Comparison with FinFET and CMOS of 14T SRAM Cell 4 bit

S.NO.	NM	Power in nW for CMOS	Power in nW for FinFET	Power in nW for GNRFET
1	22	2.81	1.35	1.17
2	14	2.36	1.26	-
3	10	1.92	1.22	-
4	7	1.82	1.19	-

Table 3: Comparison with FinFET and CMOS of 14T SRAM Cell 8 bit

S.NO.	NM	Power in nW for CMOS	Power in nW for FinFET	Power in nW for GNRFET
1	22	3.01	1.92	1.46
2	14	2.62	1.72	-
3	10	2.21	1.65	-
4	7	1.98	1.58	-

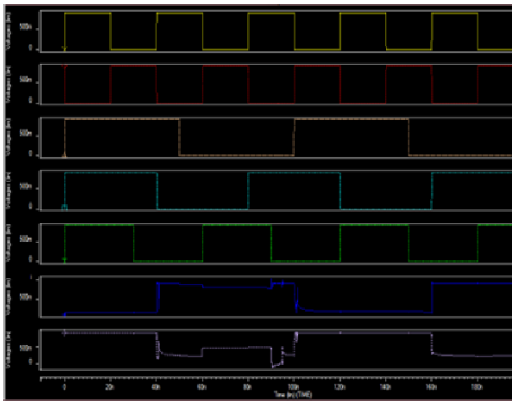

Fig 8(a)

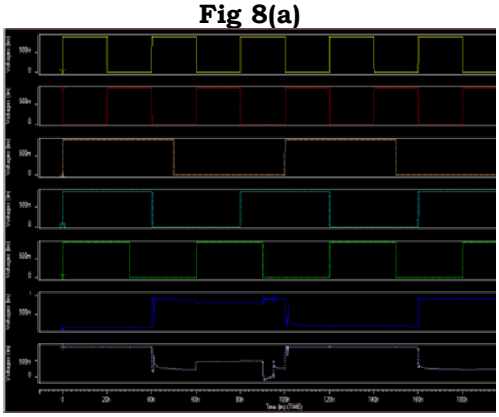

Fig 8(b)

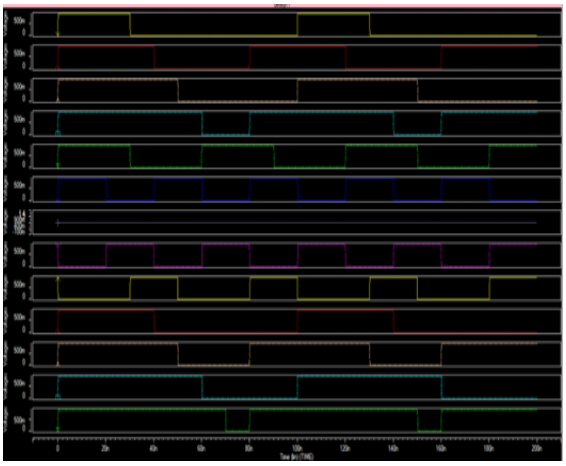

Fig 8(C)

Figure 8 Wave forms for (a) 1 bit (b) 4 bit (c) 8 bit

Table 4 Technology Parameters 22nm-1bit FinFET

S.NO.	PARAMETER	VALUE
1	Power_avg	3.5702E-05 from= 0.0000E+00 to= 2.0000E-07
2	Avgpwr	3.5989E-05 from= 5.0000E-09 to= 2.0000E-07
3	q_rise_delay	Failed
4	Trig	not found
5	Tpd	2.7406E-11
6	qn_rise_delay	2.7406E-11
7	qn_fall_delay	-2.9433E-11
8	SupplyCurrent	1.5602E-05 from= 0.0000E+00 to= 1.0000E-08
9	Static power	-7.8011E-06
10	high_low_total_energy	3.8728E-14
11	low_to_high_total_energy	3.9283E-14
12	dynamic_energy	7.8011E-14
13	total_dynamic_energy	3.9005E-14
14	total_dynamic_power	-1.2346E-29

Table 5: Technology Parameters 22nm-4 bit FinFET

S.NO.	PARAMETER	VALUE
1	Power_avg	1.3515E-09 from= 0.0000E+00 to= 2.0000E-08
2	Avgpwr	1.3515E-09
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	4.4678E-11
5	Tpd	2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	1.8714E-10

7	qn_fall_delay	3.8400E-11
8	SupplyCurrent	6.5328E-10
9	Static power	5.8795E-10
10	high_low_total_energy	5.8867E-18
11	low_to_high_total_energy	7.2297E-21
12	dynamic_energy	5.8795E-18
13	total_dynamic_energy	2.9398E-18
14	total_dynamic_power	1.2346E-29

Table 6: Technology Parameters 22nm-8 bit FinFET

S.NO.	PARAMETER	VALUE
1	Power_avg	1.9230E-09 from= 0.0000E+00 to= 3.0000E-08
2	Avgpwr	1.9230E-09
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	2.1673E-11
5	Tpd	2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11
8	SupplyCurrent	1.3066E-09
9	Static power	-1.1759E-09
10	high_low_total_energy	1.1773E-17
11	low_to_high_total_energy	-1.4459E-20
12	dynamic_energy	1.1759E-17
13	total_dynamic_energy	5.8795E-18
14	total_dynamic_power	-1.2346E-29

Table 7: Technology Parameters 22nm-1bit GNRFET

S.NO.	PARAMETER	VALUE
1	Power_avg	2.4929E-08 from= 0.0000E+00 to= 2.0000E-07
2	Avgpwr	5.8509E-08 from= 5.0000E-09 to= 2.0000E-07
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	4.0215E-08 targ= 4.0260E-08 trig= 4.4678E-11
5	Tpd	0.0000E+00 targ= 2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11 pdp= 0.0000E+00
8	Supply Current	1.6332E-10 from= 0.0000E+00 to= 1.0000E-08 staticpower= -1.4699E-10
9	Static power	-1.6748E-01
10	high_low_total_energy	1.6352E-18 from= 0.0000E+00 to= 5.0000E-09
11	low_to_high_total_energy	-1.8074E-21
12	dynamic_energy	1.4699E-18
13	total_dynamic_energy	7.3494E-19
14	total_dynamic_power	-1.2346E-29

Table 8:Technology Parameters 22nm-4 bit GNRFET

S.NO.	PARAMETER	VALUE
1	Power_avg	1.1715E-09 from= 0.0000E+00 to= 2.0000E-08
2	Avgpwr	5.8509E-08 from= 5.0000E-09 to= 2.0000E-07
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	4.4678E-11
5	Tpd	0.0000E+00 targ= 2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11
8	SupplyCurrent	6.5328E-10 from= 0.0000E+00 to= 1.0000E-08
9	Static power	-5.8795E-10
10	high_low_total_energy	5.8867E-18
11	low_to_high_total_energy	-7.2297E-21
12	dynamic_energy	5.8795E-18
13	total_dynamic_energy	2.9398E-18
14	total_dynamic_power	-1.2346E-29

Table 9: Technology Parameters 22nm-8 bit GNRFET

S.NO.	PARAMETER	VALUE
1	Power_avg	1.4630E-09 from= 0.0000E+00 to= 3.0000E-08
2	Avgpwr	1.6797E-10 from= 5.0000E-09 to= 3.0000E-08
3	q_rise_delay	3.6266E-11 targ=8.0944E-11 trig= 4.4678E-11
4	Trig	4.4678E-11
5	Tpd	0.0000E+00 targ= 2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11pdp= 0.0000E+00
8	SupplyCurrent	1.3066E-09 from= 0.0000E+00 to= 1.0000E-08
9	Static power	-1.1759E-09
10	high_low_total_energy	1.1773E-17
11	low_to_high_total_energy	-1.4459E-20
12	dynamic_energy	1.1759E-17
13	total_dynamic_energy	5.8795E-18
14	total_dynamic_power	-1.2346E-29

5 CONCLUSION

Traditional Si-CMOS technology is struggling to keep up with the demands of ever-smaller devices because to difficulties such short channel effects, higher leakage current, and process variance [35, 36]. Conventional Si-CMOS technology suffers strain as a result of modern manufacturing techniques, and its scalability is constrained by short channel effects. FinFET, silicon-on-insulator (SOI) MOSFET, and carbon-based devices have largely supplanted conventional CMOS in recent years [38–

40]. Carbon nanotube field effect transistors (CNTFETs) and graphene nanoribbon field effect transistors (GNRFETs) stand out as prospective alternatives due to their remarkable electrical characteristics and high-density capabilities, made feasible by breakthroughs in fabrication techniques. There are problems with alignment and transfer in CNTFET-based devices, but they are avoided in GNRFET-based devices [36]. Higher metal-contact resistance causes more heat to be dissipated, which is another problem with CNTFET technology. Transfer-free fabrication is an easy in situ procedure that is silicon compatible and may be used to create GNRFETs [37]. Heat dissipation, delays, and power consumption are all drastically reduced in GNRFETs compared to traditional Si-CMOS and CNTFET based devices because of their low metal-contact resistance [38]. As metal-low graphene has low contact resistance, it can be used in high-speed electronic devices and is hence a potential component in high-speed memory circuits. However, advancement is hindered by the fact that graphene-based transistors have an unstable conductivity as a result of manufacturing changes and a zero bandgap [39, 40]. To ensure that graphene nanoribbon FET memory circuits can function in practical contexts, it is necessary to assess these effects.

REFERENCES

1. Mihir R. Choudhury, *Student Member, IEEE*, Youngki Yoon, *Member, IEEE*, Jing Guo, *Member, IEEE*, and Kartik Mohanram, *Member, IEEE* "Graphene Nanoribbon FETs: Technology Exploration for Performance and Reliability", IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 10, NO. 4, JULY 2011
2. Divya Geethakumari Anil, Yu Bai and Yoonsuk Choi, "Performance Evaluation of Ternary Computation in SRAM Design Using Graphene Nanoribbon Field Effect Transistors" 978-1-5386-4649-6/18/ ,2018, IEEE
3. Performance Evaluation of A Low Transistor Ternary CNTFET SRAM Cell", IEEE Conference on Electronic Design, Computer Networks & Automated Verification (EDCAV), January 2015.
4. S. Lin, Y. B. Kim, and F. Lombardi, "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits", IEEE Transactions on Nanotechnology, Vol. 10, No. 2, March 2011.
5. P. Wessely, F. Wessely, E. Birinci, U. Schwalke, and B. Riedinger, "Transfer-free Fabrication of Graphene Transistors," J. Vac. Sci. Technol. B 30, 2012.
6. A. Murugesan, "A Theoretical description of Graphene based Transistors", IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 1 Issue 3, May 2014.
7. A. Imran, R. S. Singh, M. Mishra, "Simulation Study of Logic Circuits using Optimized Graphene Nanoribbon Fets ", 2016 2nd International Conference on Next Generation Computing Technologies (NGCT-2016) Dehradun, India 14-16 October 2016.
8. R. T. Greenway, K. Jeong, A. B. Kahng, C. H. Park, and J. S. Petersen,"332nm 1-D Regular Pitch SRAM Bitcell Design for Interference-Assisted Lithography", Proceedings Volume 7122, Photomask Technology 2008
9. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, pp. 666–669, 2004.
10. Y. Zhang, Y.-W. Tan1, H. L. Stormer, and P. Kim, "Experimental observation of the quantum Hall effect and Berry's phase in graphene," *Nature*, vol. 438, pp. 201–204, 2005.
11. C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N.Marchenkov, E. H. Conrad, P. N. First, andW. A. de Heer, "Electronic confinement and coherence in patterned epitaxial graphene," *Science*, vol. 312, pp. 1191–1196, 2006.
12. R. V. Noorden, "Moving towards a graphene world," *Nature*, vol. 442, pp. 228–229, 2006.
13. A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Mater.*, vol. 6, pp. 183–191, 2007.
14. W. A. de Heer, C. Berger, E. Conrad, P. First, R. Murali, and J. Meindl, "Pionics: The emerging science and technology of graphene-based nanoelectronics," in *Intl. Electron Devices Meeting Tech. Dig.*, 2007, pp. 199–202.
15. Z. Chen, Y.-M. Lin,M. J. Rooks, and Ph. Avouris, "Graphene nano-ribbon electronics," *Physica E: Low-dimensional Syst. Nanostruct.*, vol. 40, pp. 228–232, 2007.
16. M. Y. Han, B. O¨ zyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.*, vol. 98, pp. 206805- 1–206805-4, 2007.
17. X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultra smooth graphene nanoribbon semiconductors," *Science*, vol. 319, pp. 1229–1232, 2008.
18. Y.-W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in grapheme nanoribbons," *Phys. Rev. Lett.*, vol. 97, pp. 216803-1–216803-4, 2006.
19. K. S. Novoselov et al., "Electric field effect in atomically thin carbon films," Science, vol. 306, pp. 666–669, 2004.
20. Y. Zhang et al., "Experimental observation of the quantum Hall effect and Berry's phase in graphene," Nature, vol. 438, pp. 201–204, 2005.
21. C. Berger et al., "Electronic confinement and coherence in patterned epitaxial graphene," Science, vol. 312, pp. 1191–1196, 2006.

22. R. V. Noorden, “Moving towards a graphene world,” Nature, vol. 442, pp. 228– 229, 2006.
23. X. Li et al., “Chemically derived, ultrasmooth graphene nanoribbon semiconductors,” Science, vol. 319, pp. 1229–1232, 2008.
24. Niraj K. Jha, Deming Chen, “Nanoelectronic Circuit Design", Springer, 2011.
25. C. R. Manoj, Meenakshi Nagpal, Dhanya Varghese, and V. Ramgopal Rao, " Device Design and Optimization Considerations for Bulk FinFETs", IEEE transactions on electron devices, Vol. 55, No. 2, pp. 609-615, February 2008.
26. Joerg Appenzeller, "Carbon nanotubes for high performance electronics - Progress and prospect", Purdue e-Pubs, 2008.
27. Sang Hoon Chae, Young Hee Lee, “Carbon NanoTubes and graphene towards soft electronics,” Nano Convergence 2014, pp.1-15.
28. Narender Hanchate & N. Ranganathan, (2004),’A New Technique for Leakage Reduction in CMOS Circuits using Self-Controlled Stacked Transistors”, Proceedings of the 17th International Conference on VLSI Design (VLSID”04) IEEE.
29. Z. Chen, Y.-M. Lin,M. J. Rooks, and Ph. Avouris, “Graphene nano-ribbon electronics,” *Physica E: Low-dimensional Syst. Nanostruct.*, vol. 40, pp. 228–232, 2007.
30. M. Y. Han, B. O¨ zyilmaz, Y. Zhang, and P. Kim, “Energy band-gap engineering of graphene nanoribbons,” *Phys. Rev. Lett.*, vol. 98, pp. 206805- 1–206805-4, 2007.
31. X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, “Chemically derived, ultra smooth graphene nanoribbon semiconductors,” *Science*, vol. 319, pp. 1229–1232, 2008.
32. Y.-W. Son, M. L. Cohen, and S. G. Louie, “Energy gaps in grapheme nanoribbons,” *Phys. Rev. Lett.*, vol. 97, pp. 216803-1–216803-4, 2006.
33. K. S. Novoselov et al., “Electric field effect in atomically thin carbon films,” Science, vol. 306, pp. 666–669, 2004.
34. Y. Zhang et al., “Experimental observation of the quantum Hall effect and Berry’s phase in graphene,” Nature, vol. 438, pp. 201–204, 2005.
35. C. Berger et al., “Electronic confinement and coherence in patterned epitaxial graphene,” Science, vol. 312, pp. 1191–1196, 2006.
36. R. V. Noorden, “Moving towards a graphene world,” Nature, vol. 442, pp. 228– 229, 2006.
37. X. Li et al., “Chemically derived, ultrasmooth graphene nanoribbon semiconductors,” Science, vol. 319, pp. 1229–1232, 2008.
38. Niraj K. Jha, Deming Chen, “Nanoelectronic Circuit Design", Springer, 2011.
39. C. R. Manoj, Meenakshi Nagpal, Dhanya Varghese, and V. Ramgopal Rao, " Device Design and Optimization Considerations for Bulk FinFETs", IEEE transactions on electron devices, Vol. 55, No. 2, pp. 609-615, February 2008.
40. Joerg Appenzeller, "Carbon nanotubes for high performance electronics - Progress and prospect", Purdue e-Pubs, 2008.
41. S. Banerjee, M. Sardar, N. Gayathri, A. K. Tyagi, and B. Raj, “Enhanced conductivity in graphene layers and at their edges,” *Appl. Phys. Lett.*, vol. 88, no. 6, pp. 62 111-1–62 111-3, Feb.2006.
42. B. J. Sheu, D. L. Scharfetter, P. K. Ko, and M. C. Jeng, “BSIM: Berke- leyshort-channel IGFET model for MOS transistors,” IEEE J. Solid- State Circuits, vol. SC-22, pp. 558–566, Aug. 1987.
43. Narender Hanchate, Nagarajan Ranganathan, “LECTOR: A Technique for Leakage Reduction in CMOS Circuits”, IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 12, No. 2, February 2004.